Amendments to the Specification:

Please replace the heading beginning at page 1, line 3, with the following redlined paragraph (or section):

~~FIELD OF INVENTION~~ BACKGROUND OF THE INVENTION

Field of the Invention

Please delete the section beginning at page 1, line 16 and ending at page 2, line 8.

Please add, beginning at page 2 between lines 8 and 9, the following new heading:

Description of the Related Art

Please delete the heading at page 3, line 21.

Please add, beginning at page 11 between lines 17 and 18, the following new section:

BRIEF SUMMARY OF THE INVENTION

The invention relates to an area-efficient realization of a coefficient block with hardware sharing techniques and optimizations applied to this block. The block is connected to coefficient lines coming from a delay block to be connected to perform a filtering operation or a mathematical computing operation with optimization in hardware and provides a zero latency output. The invention also gives the area minimal realization of digital filters based on the coefficient block, when operated in serial bit fashion. The optimization techniques and structure of the present invention are good for bit-serial digital filters typically a finite impulse response (FIR) filter, including finite impulse response filter (IIR) and for other filters and applications based on combinational logic that includes delay elements, multipliers, and serial adders and/or subtractors.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Figure 1 shows the field of the invention and applications of the device.

Figure 2 shows the symbol of components used in the device.

Figure 3 shows the description of components used in the device.

Figure 4 shows bit-serial FIR filter implementations.

Figure 5 shows an example of a FIR filter.

Figure 6 shows one of the known minimization technique due to symmetry of coefficients.

Figure 7 shows the structure of a prior/known implementation technique for a coefficient block.

Figure 8 shows the generalized structure of a prior/known implementation technique for a coefficient block.

Figure 9 shows the minimization technique involved in a FIR filter.

Figure 10 shows the generalized structure of the minimization technique involved in the FIR filter.

Figure 11 shows the minimized structure of this example FIR filter, of the present invention.

Figure 12 shows the generalized optimized structure of the present invention.

Figure 13 shows the other advantage of the structure, i.e., getting the parallel output directly, of the present invention.